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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,764	10/09/2001	Harry Dwyer	Dwyer 5-13	9496

7590 10/20/2006

Ryan, Mason & Lewis, LLP
Suite 205
1300 Post Road
Fairfield, CT 06430

EXAMINER	
LANE, JOHN A	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 10/20/2006

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/975,764
Filing Date: October 09, 2001
Appellant(s): DWYER ET AL.

Kevin M. Mason
For Appellant

EXAMINER'S ANSWER

This examiner's answer is responsive to the corrected appeal brief filed 01/24/2006 appealing from the Office action mailed 08/30/2004. Appellant was contacted on 10/11/05 and 10/18/05 regarding the allowability of claims 9 and 10. Appellant declined to make the necessary amendment to place the application in condition for allowance.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claim 1-8 and 11-36.

Claims 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

No amendments after have been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,353,425	Malamy	10-1994

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-8 and 11-36 are rejected under 35 U.S.C. section 103(a) as being unpatentable over the admitted prior art in view of Malamy et al. (Pat. No. 5,353,425).

The admitted prior art found on pages 1-3 of the present specification teaches a cache for storing a plurality of frames from main memory. The claimed step of "locking frames if a task is interrupted by another task" corresponds to the locking of an executing task's frames prior to an interruption from another task's execution (page 2, lines 8-10). However, locking a frame or frames in accordance with a most recently used scheme is not discussed.

Malamy is introduced as teaching locking pages or blocks in a cache in accordance with a most recently used locking scheme. As shown in figure 4c an MRU bit (essentially a lock bit) locks a cache line or lines in accordance with a most recently used locking scheme. This scheme increases operating speed, requires less complex logic than a LRU scheme and does not require much high-speed cache memory to implement (col. 3, lines 6-13).

Because the most recently used locking scheme of Malamy provides for an increase in operating speed and reduction in complexity it would have been obvious to use such a locking scheme to lock the frames/blocks/pages/lines of the cache device of the admitted prior art. Therefore, the claimed invention would have been obvious to one of ordinary skill in the art at the time of the invention.

Appellant should also consider that present independent claims 1, 15, 23, 29 and 33 do not preclude locking all frames of a task. That is, a broad interpretation of the claims includes locking the most recently used frames and the remaining frames

associated with a task. Given this interpretation, the admitted prior art would clearly read on the independent claims since all frames of a task are locked including the most recently used frames.

The examiner believes all dependent claim features are either expressly or inherently taught by the admitted prior art and/or Malamy.

In the brief filed 01/24/2006 appellant presents - for the first time - arguments directed to dependent claims 5, 6, 11, 13, 18, 19, 24, 25, 31 and 34-36. The examiner has addressed the new arguments in section 10 below and incorporated the discussion of the dependent claims in the art rejection of this section.

Claims 5 and 18 recite, "said identifier of the n most recently used frames is maintained for each of a plurality of tasks." The admitted prior art (page 2 of spec.) teaches:

> [E]xecution of a special instruction or by writing to a memory mapped control register that may **control groups of frames** or individual frames. The **locking of some of an executing task's frames** prior to another task's execution ensures that blocks in those frames are not evicted. This may enhance the performance of the interrupted task when it resumes execution.

The admitted prior art essentially teaches the concept of associating frames with one of a plurality of tasks. This is seen in the statement "locking of some of an executing task's frames prior to another task's execution ensures that blocks in those frames are not evicted." Thus, the concept of selectively locking some frames associated with a task is well known. Maintaining a relationship of frames to tasks is also well known.

Claims 6, 19, 24 and 34 recite, "said adaptive frame locking mechanism does not lock all the frames in a set concurrently." The examiner contends the frames in either the admitted prior art or Malamy can be locked over time (i.e. not concurrently) as needed. That is, Malamy's device determines which MRU frames/lines/blocks to lock over time.

Claims 7 and 20 recite, "said number of said most recently used frames identifies the most recently accessed 3n/2 frames on average." Appellant should note the variable "n" is not limited to a specific number or range. A value of 2/3 for n would yield 1 in the equation 3n/2. The examiner contends Malamy teaches at least 1 most recently used frame or most recently accessed frame on average.

Claims 11, 25, 31 and 35 recite, "an adaptive frame unlocking mechanism that automatically unlocks frames that cause a performance degradation for a task." Malamy teaches resetting a lock bit in accordance with a locking scheme that controls the state of lock bits based upon the intelligence and knowledge of frequency of use of certain memory locations to provide a more efficient cache (see Abstract).

Claims 13 and 36 recite, "said cache is a two way set associative cache and said most recently used frames are identified by taking an inverse of a least recently used identifier." Malamy teaches a Pseudo-Least-Recently-Used (PLRU) scheme that uses a MRU bit that indicates the cache memory line has been used recently (col. 3, lines 6-19). Thus, a set LRU bit would not identify the most recently used (MRU) frame/block/line and a set MRU bit would not identify the least recently used (LRU) frame/block/line. Furthermore, Malamy (see Summary) discusses fully associative, set associative and

direct mapped caches. A two way set associative cache is inherently within the scope of Malamy's invention.

(10) Response to Argument

In the Argument section of the brief, appellant argues the following with respect to independent claims 1, 15, 23, 29 and 33:

> [T]he admitted prior art and Malamy, alone or in combination, do not disclose or suggest locking a number of most recently used frames associated with a task...or...if a task is interrupted by another task

Appellant further argues:

> [T]he admitted prior art teaches away from the present invention by teaching to lock **all** frames associated with a task.

and;

> Malamy, therefore, actually teaches away from the present invention by teaching to block the replacement of the most recently used cache lines **regardless of the task they are associated with**

In response, appellant does not consider the synergy that arises in the combination of the admitted prior art and Malamy. That is, appellant does not consider the benefits of both prior art devices working in concert. The examiner contends that each prior art device working together would lock the most recently used frames of a task. The admitted prior art would identify the frames/blocks/lines associated with a task and the device of Malamy would select only the most recently used frames/blocks/lines to be locked for a task. One skilled in the art is motivated to use the MRU locking scheme of Malamy in the device of the admitted prior art because such a combination would result

in a faster more efficient cache (Summary of Malamy) and faster processing of frames associated with a task.

In the brief filed 01/24/2006 appellant presents - for the first time - arguments directed to dependent claims 5, 6, 11, 13, 18, 19, 24, 25, 31 and 34-36. The examiner has addressed the new arguments below and incorporated the discussion of the dependent claims in the art rejection of section 5.

Appellant further argues:

> Claims 5 and 18 require an identifier of the n most recently used frames is maintained for each of a plurality of tasks.

In response, the admitted prior art (page 2 of spec.) teaches:

> [E]xecution of a special instruction or by writing to a memory mapped control register that may **control groups of frames** or individual frames. The **locking of some of an executing task's frames** prior to another task's execution ensures that blocks in those frames are not evicted. This may enhance the performance of the interrupted task when it resumes execution.

The admitted prior art essentially teaches the concept of associating frames with one of a plurality of tasks. This is seen in the statement "locking of some of an executing task's frames prior to another task's execution ensures that blocks in those frames are not evicted." Thus, the concept of selectively locking some frames associated with a task is well known. Maintaining a relationship of frames to tasks is also well known.

Appellant further argues:

> Claims 6, 19, 24, and 34 require not locking all the frames in a set concurrently.

In response, the examiner contends the frames in either the admitted prior art or Malamy can be locked over time (i.e. not concurrently) as needed. That is, Malamy's device determines which MRU frames/lines/blocks to lock over time.

Appellant further argues:

> Claims 7 and 20 require wherein said number of said most recently used frames identifies the most recently accessed 3n/2 frames on average.

In response, appellant should note the variable "n" is not limited to a specific number or range. A value of 2/3 for n would yield 1 in the equation 3n/2. The examiner contends Malamy teaches at least 1 most recently used frame or most recently accessed frame on average.

Appellant further argues:

> Claims 11, 25, 31, and 35 require an adaptive frame unlocking mechanism that automatically unlocks frames that cause a performance degradation for a task.

In response, Malamy teaches resetting a lock bit in accordance with a locking scheme that controls the state of lock bits based upon the intelligence and knowledge of frequency of use of certain memory locations to provide a more efficient cache (see Abstract).

Appellant further argues:

> Claims 13 and 36 require wherein said cache is a two way set associative cache and said most recently used frames are identified by taking an inverse of a least recently used identifier.

In response, Malamy teaches a Pseudo-Least-Recently-Used (PLRU) scheme that uses a MRU bit that indicates the cache memory line has been used recently (col. 3, lines

6-19). Thus, a set LRU bit would not identify the most recently used (MRU) frame/block/line and a set MRU bit would not identify the least recently used (LRU) frame/block/line. Furthermore, Malamy (see Summary) discusses fully associative, set associative and direct mapped caches. A two way set associative cache is inherently within the scope of Malamy's invention.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Jack Lane

Conferees:

DONALD SPARKS
SUPERVISORY PATENT EXAMINER

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100